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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,835	03/30/2004	Kazuaki Goto	030712-29	3051

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EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	**PAPER NUMBER**
2825	

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12/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/811,835	GOTO ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/29/2007, 10/12/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *6-9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 10-13* is/are rejected.

7)☒ Claim(s) *4,5,14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/811,835 filed 03/30/2004 and amendment filed 06/29/2007 and Response to Election/Restriction filed 10/12/2007.

2. Claims 1-15 remain pending in the Application. Based on Response to Election/Restriction claims 1-5 and 10-15 remain under consideration for further examination and claims 6-9 are withdrawn from consideration as non-elected claims.

3. Applicant's arguments filed 06/29/2007 have been fully considered but they are not persuasive.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

5. Claims 1 and 10 are objected to because of the following informalities:

Claim 1 line 6 after "interconnect" delete "patters" insert –patterns--

Claim 10 line 6 after "interconnect" delete "patters" insert –patterns--

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 10-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Solomon et al. (US Patent 6,446,248).

With respect to claim 1 Solomon et al. teaches a method of designing a circuit layout of a semiconductor integrated circuit (abstract), comprising:

designing a logic function of the integrated circuit within inserting a standard cells as shown on the Fig. 4 (col. 7, ll.20-21), wherein during integrated circuit design standard cells are pre-designed and configured to perform a predetermined function (col. 4, ll.64-65);

designing a pattern layout of the integrated circuit so that the pattern layout includes a logic cell area and an open area as shown on the Fig. 4, wherein integrated circuit layout includes logic cells (standard cells) to determine the function of the integrated circuit and unused areas (open) 401, 402, 403, 404, 405, 406 (col. 7, ll.19-21);

providing a spare underground cell having no interconnect patterns and contacts (within base cells 245 shown on the Fig. 3A, wherein base cell 245 includes plurality of transistors that have unconnected terminals (no interconnect patterns and contacts) (col. 5, ll.10-16));

inserting the spare underground cell into the open area, wherein the spare underground cell includes a functional element (within inserting base cells 245 into the circuit design layout into unused area in the circuit design layout (col. 7, ll.9-12), wherein base cell 245 implemented with different types of functional elements, such as different types of transistors and their combinations (col. 7, ll.37-46)); and

designing a mask layout of the integrated circuit, the mask layout including the logic cell and the spare underground cell (within fabrication stage/masking of the integrated circuit design, wherein the integrated circuit layout includes logic/standard cells 235 and spare underground/base cells 245 (col. 6, ll.43-47)).

With respect to claim 10 Solomon et al. teaches limitations similar to the limitations of the claim 1 including plurality of logic cells and plurality of spare underground cells in the integrated circuit layout design as shown on the Figs. 2, 4 (col. 6, ll.43-47).

With respect to claims 2-5, 11-15 Solomon et al. teaches:

Claims 2, 11: wherein the functional element includes a D flip-flop, an inverter, a NOR circuit, a NAND circuit an exclusive OR circuit and a latch circuit (col. 5, ll.14-16);

Claims 3, 13: wherein inserting the spare underground cell includes:

dividing the pattern layout into a plurality of block regions (within partitioning the layout of the integrated circuit into blocks as shown on the Fig. 4 (col. 2, ll.50-51);

searching the open area from the block regions by searching and extracting empty spaces, i.e. unused by standard cells (col. 4, ll.23-24));

distributing the open area into the block regions (col. 7, ll.21-22); and

inserting the spare underground cell into the distributed open area (using area-based placement routing tool for placing ponds of gates (POGs) 411-416 as shown on the Fig. 4A (col. 7, ll.25-26), wherein POGs are sets of base cells (spare) (col. 7, ll.28-29));

Claim 12: wherein each of the spare underground cells has a same kind of the functional elements (col. 5, ll.14-16; col. 7, ll.37-46).

Allowable Subject Matter

8. Claims 4, 5, 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach setting a flag when all inserting within the attended block region are finished among with all limitations of the claims 4 and 14 and claims 1 and 10, from which they depend.

Remarks

9. In remarks Applicant argues in substance:

a) Solomon et al. reference clearly fails to disclose or remotely suggest that the base cell 245 has no interconnect patterns and contacts

b) Solomon et al. shows that the base cell 245 includes interconnect patterns, that being the metal traces and contacts.

10. Examiner respectfully disagrees for the following reasons:

With respect to a) Solomon et al. teaches base cells 245 as shown on the Fig. 3A, wherein architecture of the base cell 245 depicted as plurality of unconnected transistors, wherein no interconnect patterns and contacts are shown (col. 5, ll.10-16). Therefore Examiner believes that the term in the newly added limitation of the claims 1 and 10 "spare underground cell having no interconnect patterns and contacts" is

equivalent to having unconnected terminals of the transistors of base cell 245 (col. 5, ll.10-11).

With respect to b) it has to be noted that in this argument Applicant's representative cited description of the Fig. 3B, which is a physical layout of the base cell 245 and discloses process of fabricating stage of the integrated circuit including base cell, wherein Solomon et al. teaches fabrication stage of the integrated circuit design layout including adding metal layers 1 and 2 to the base cell 245 layout, which shown on the Fig. 3B.

Based on at least these disclosures of Solomon et al. Examiner maintains rejection of claims 1-3, 10-13 under 35 USC § 102.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HR
11/30/2007

Examiner Helen Rossoshek
/Helen Rossoshek/
Art Unit 2825